M.S. Thesis

A Multi-Segmented LED Driver with LUT-Based Control using Background Calibration

백그라운드 교정기술을 이용한 룩업테이블 제어방식이 적용된 분할 엘이디 드라이버

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August 2017

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A Multi-Segmented LED Driver with LUT-based control using Background Calibration

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A thesis submitted to the department of electrical and computer engineering

August 2017

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August 2017

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Abstract

Light-emitting diode (LED) lighting is becoming a major illumination method with supports from global energy institutions such as department of energy (DOE) in the United States. It is because LED replacement can save a lot of global energy consumption due to its superior efficacy over conventional light sources. However, for a rapid adoption of LED lighting, lower cost and reliable driver is required.

This thesis presents an AC-powered, boost-converter-based multi-segmented LED driver that maintains a high-power factor (PF) and accurate input current level, using a novel look-up table (LUT)-based digital control with a simple predictive duty-cycle control scheme and background calibration. The presented multi-segmented LED driver aims to reduce the costs of high-voltage capacitors and high-inductance inductor by segmenting the load LEDs into multiple strings and switching the number of LED strings which are connected in series for line regulation and power-factor correction. However, the increased number of power switches calls for a sophisticated control scheme that responds quickly to the switching mode changes and adapts properly to the operating condition changes.

The presented LED driver addresses this by employing a LUT that can provide a pre-programmed, arbitrarily fast response to the periodic 220-V AC input, supplemented by a periodic background calibration and optimal switching mode selection to track any unexpected changes in the input, load, and environment conditions. A prototype 220-V AC LED driver with 6-segment LED strings

demonstrates a 98.4% power factor (PF), 91% conversion efficiency, 26 mA_{rms} input current error, and 67% reduction of discrete component costs while delivering 38.3-W to the load.

Keyword: AC-powered LED Driver, Predictive Control, Lookup-table (LUT), Boost Converter, Segmentation

Student Number: 2014-22575

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Chapter 1
Introduction

1.1. AC-powered LED Driver

There is a strong demand for low-cost, high-efficiency AC-powered LED drivers that also meet the mandated industrial standards such as IEC 61000-3-2 [1]. One reason for the high cost of the existing LED drivers is the use of costly passive components. Especially when operating off of a 220-V AC input of which peak instantaneous voltage can reach above 300V, a high-voltage capacitor or high-inductance inductor is typically required to filter the voltage or current, respectively. To address this issue, a multi-segmented LED driver adopting a multi-level converter topology was previously presented [2] to exploit the fact that it is more cost-effective to use multiple low-voltage capacitors than a single high-voltage capacitor. However, the sudden changes in the switching mode and also in the duty-cycles required for the power switches render the conventional linear feedback controls in [3] – [6] ineffective. Leveraging the fact that the AC power input to the LED driver is periodic, previous work [7] reported an improved multi-segmented driver employing a look-up table (LUT) based digital controller with background calibration and optimal switching mode selection schemes. This thesis presents a more detail analysis on the operation of the proposed LED driver in [7]. As a result, the prototype LED driver with 6-segment LED strings demonstrates a

98.4% power factor (PF), 91% conversion efficiency and 67% reduction of discrete component costs.

Among the previously presented LED drivers at competitive price in [2] – [4], this thesis adopts a boost-converter-based topology [2] and maximizes its price competitiveness. First, it can perform both power factor correction (PFC) and regulation just by a single stage converter which has advantages of cost reduction and high conversion efficiency compared to the conventional two-stage schemes [5] – [6]. Second, in contrast to the previous buck-boost [3] or flyback [4] converter-based schemes, it ensures the continuous and non-pulsating input current so that a bulky input EMI filter, which takes considerable portion in unit price, is unnecessary. Third, the burden on a high output voltage can be alleviated by simply segmenting an LED string into multiple sections, which minimizes discrete component costs and reduces the inductance and the voltage rating of the output capacitors.

Considering these benefits, this thesis suggests a background look-up table (LUT)-calibration and a flexible switching mode alternation technique for an LUT-based control that can perform intricate calibration and precise control just by a low-cost, single IC. While using AC-powered applications, various LUT-based control schemes have been able to simply perform PFC in a condition of fixed, periodic input voltage (i.e., 50/60-Hz) [8] – [9]. However, because I-V characteristic of LEDs is susceptible to temperature variation, the proposed scheme senses a present status of a current error, which is the difference between an

inductor current and that in a pre-configured LUT, and calculates a compensated duty-cycle ratio through an LUT calibration logic. Accordingly, instead of fully scheduling the number of connected switches before the operation, a hysteretic control-based feedback loop continuously calibrates the LUT so that the renewed duty-cycle ratios controlling the switches reflect the actual LED voltages. Meanwhile, a switching mode selector determines an optimal switching mode to provide minimized load voltage across the inductor, which enables the use of a low-inductance inductor. In this scheme, smooth transition of an out-bounded switching mode to a neighbor prevents PFC failure at near-mode-boundaries, especially when voltage ripples and temperature drift exist. As a result, it is more resilient to non-ideality of voltage across the LEDs, and no longer requires excessively large capacitors to eliminate voltage ripples.

1.2. Thesis Organization

The rest of this paper is organized as follows. Chapter 2 describes the overall architecture of the proposed LED driver with cost optimization based on the market price. Chapter 3 illustrates the detail techniques for switching scheduling which can be applied in case of segmented boost converter. Chapter 4 describes duty-cycle control method of proposed LED driver including LUT calibration and switching mode alternation scheme. Finally, chapter 5 presents the measurement results of the prototype 220-V LED driver, and chapter 6 concludes the paper.

Chapter 2
Multi-Segmented LED Driver Architecture

2.1. Multi-Segmented Boost Converter Topology

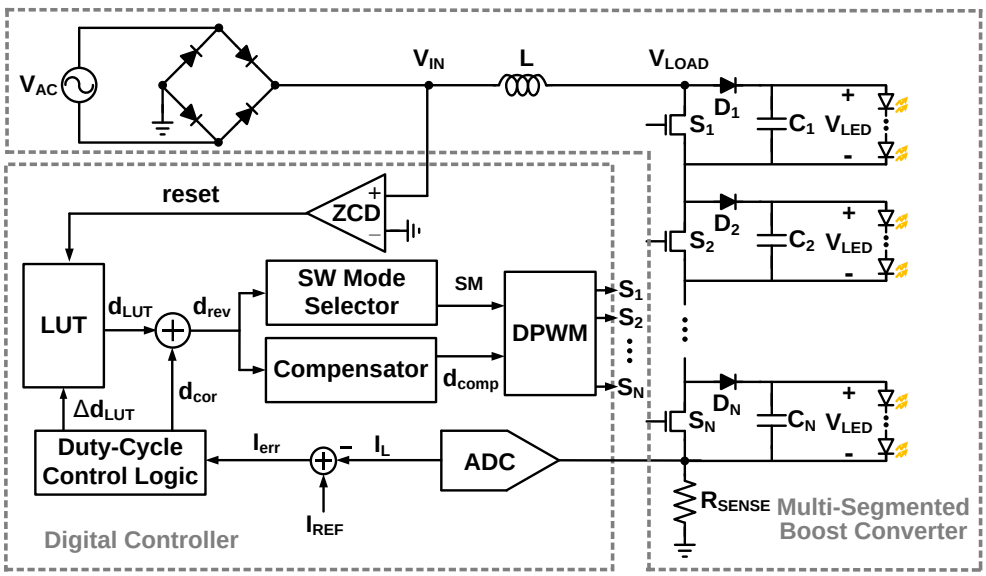

Fig. 2.1. The overall architecture of the multi-segmented LED driver and block diagram of the digital control scheme.

The overall architecture of the proposed LED driver is shown in Fig. 2.1. The proposed LED driver employs an AC-DC boost converter including *N*-segmented LED sections and control switches (S_1, S_2, …, S_N) as a power stage and a LUT-based digital controller. The topology of a half-bridge modular multilevel converter [10] – [11], which is widely used for high voltage direct current (HVDC)

transmission, is applied to the boost converter.

The component constraints such as voltage rating of capacitors and inductance in the boost converter are alleviated through dividing load into multiple sections. A basic boost converter (i.e., N=1) is not suitable for high voltage application because the maximum output voltage is higher than that of input voltage, requiring capacitor/switch that can endure it. For example, voltage rating of those components should be at least 300-V when the input voltage is 220-V. On the other hand, lower-voltage capacitors can be used in multi-segmented case (i.e., $N > 1$), since each string voltage is inversely proportional to the number of LED strings (N). Also, a low-inductance inductor is employed by introducing proposed digital control scheme that will be described in detail in following chapters. Briefly, lower voltage is applied to the inductor than basic booster converter (nearly 1/N times) because the control scheme maintains the total load voltage (V_{LOAD}) to be switched near the input voltage level (V_{IN}). To regulate input current ripple constantly, 1/N times reduced inductance can be used minimally. And it can be shown with following equation,

$$\Delta i_L = \frac{\Delta V_L}{L_s} \cdot \Delta t = \frac{\Delta V_L / N}{L_s / N} \cdot \Delta t = \frac{\Delta V_L / N}{L_m} \cdot \Delta t \qquad (1)$$

where Δi_L is input current ripple, ΔV_L is inductor voltage, L_s is inductance of single stage case, and L_m is inductance of multi-stage case. Also, its multi-level converter circuit topology has been conventionally used in high voltage direct current (HVDC) transmission [10] – [14], and its applicability to an LED driver has been described in [2] and [3].

2.2. LUT-Based Digital Control

A LUT-based digital control is presented to respond to the fast and periodic rectified input voltage, and to cover multiple switching modes defined as a certain number of on-state switches among *N* switches. As the number of section increases, controlling several switches simultaneously and sophisticatedly becomes significant for a stable PFC operation. The digital control consists of a look-up table (LUT), a switching (SW) mode selector, a range compensator, a digital pulse-width modulator (DPWM), a zero-crossing detector (ZCD), and an analog-to-digital converter (ADC), a duty-cycle control logic. The flow of the control is as follows. The LUT in Fig. 2.1 contains 8-bit digital codes representing the optimal duty-cycle ratios with respect to the switching modes and the input voltage levels. The DPWM modulates gate control pulse width basically in reference to the LUT and assign each signal into the switches on the base of the data from SW mode selector and a range compensator. And it also distributes gate signals to maintain current balance between each string. The SW mode selector determines the right switching mode and the range compensator performs refinement processing of the revised duty-cycle ratios in order to keep them within the valid control region, from 0 to 1, all the time. Meanwhile, the duty-cycle sequence in the LUT is reset at every detection of the zero-crossing detector (ZCD) observing 120-Hz, full-bridge rectified V_{IN}. By sensing the input current using the analog-to-digital converter (ADC) along with sense resistor (R_{sense}), it corrects the duty cycle ratios to adapt to environment change and to compensate non-ideality through the duty-cycle control

logic. After all, the LUT is under background calibration to guarantee accurate pursuit of the optimal duty-cycle ratios in the presence of temperature variation and voltage ripple. Further explanation and effectiveness on the LUT calibration and the switching mode selection tactics are illustrated in chapter 3 and 4.

2.3. Optimizing Component Cost

Upon the proposed architecture, this thesis further analyzes a relationship between the total cost of the discrete components and the number of the segments (N) to determine the optimal number of the LED segments with given input voltage level, as shown in Fig. 2.2. In terms of mass production, the digital controller and the switches can be integrated into an inexpensive single chip, while the cost of inductor and capacitors cannot be reduced and thereby significantly contribute to the unit cost. Since the required inductance of the inductor and maximum voltage rating of the capacitors decrease as the number of the LED sections increases, there exists an optimal point to minimize the total unit price. Fig. 2.2 shows component costs based on the list of market prices of discrete components (5000 E.A. standard) in Digi-Key [15] and reveals that the case of $N = 6$ is optimal assuming 220-V AC input voltage. This can make at least 67% reduction of the component costs compared to the case using a single section. Furthermore, the effectiveness of the cost reduction against the previous architectures [3] – [4] is maximized in the case of high power applications, such as streetlight, because high-inductance inductors and high-voltage-rated capacitors have been recognized as burdensome.

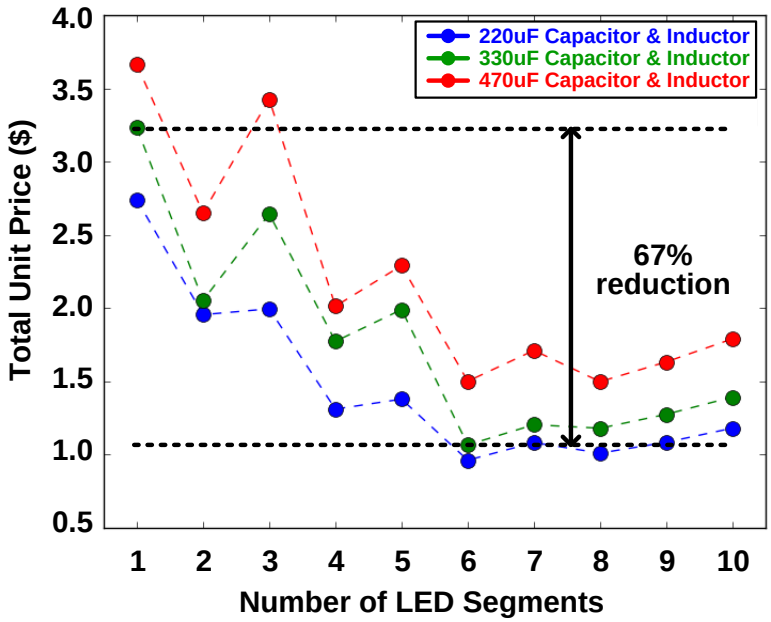

Fig. 2.2. The total discrete component costs according to the number of the LED segments.

Chapter 3
Switching Scheduling

This chapter describes the switching schedule of the switchable *N*-segmented LED driver that can reduce discrete component cost and the current balancing between LED strings. The detailed explanation of the switch scheduling includes the definition of switching mode, operation of the time division multiplexing scheme and switch schedule allocation.

3.1. Switching Mode in *N*-Segmented LED Driver

While segmenting a single LED string into *N*-section can make use of the low-cost and low-voltage-rated capacitors, *N* switching modes of the driver guarantee the inductor voltage to be nearly 1/*N* times than a single-segment case. *N* switching modes are classified by the level of the full-bridge rectified AC input voltage, V_{IN}. Fig. 3.1 illustrates the *N*-segmented LED driver at a *k*-th switching mode, assuming that the DC voltage of each LED string is V_{LED}. There are *N* switching modes during one half-line period. Each switching mode (e.g. *k*-th) is selected when the rectified AC input V_{IN} is between $(k\text{-}1)V_{LED}$ and kV_{LED} (in case $k=N$, between $(N\text{-}1)V_{LED}$ and V_m). In this *k*-th switching mode, (*k*-1) switches turn off, and (*N*-*k*) switches turn on, and the only one switch is duty-controlled switching. Such a switching schedule can keep the voltage across the inductor low

since the output load voltage switches between (k-1)V_{LED} and kV_{LED}, which are near the input voltage, V_{IN}. This reduced voltage across the inductor can reduce the inductance. Note that it can prevent crowbar current that can degrade the efficiency since only one switch is switching at a time.

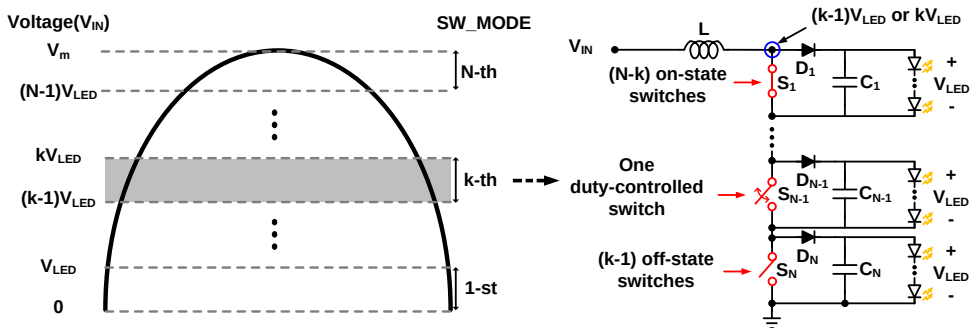

Fig. 3.1. (a) Classification of N switching modes according to the input voltage, V_{IN}, and (b) the switching state of N switches at k-th switching mode.

To help understanding of the specific switching operation, an example of 3-segmented switchable LED strings with three switching modes is illustrated in Fig. 3.2. The switching mode 1 is configured when V_{IN} is between 0 and V_{LED}. For instance, only one switch S_2 is switching and the other switches keep turned on. The switching mode 2 is configured when V_{IN} is between V_{LED} and $2V_{LED}$. For instance, only one switch S_2 is switching, S_1 turns on, and S_3 turns off. The switching mode 3 is configured when V_{IN} is between $2V_{LED}$ and $3V_{LED}$. For instance, only one switch S_2 is switching and the other switches turn off. In all the switch modes, the N-segmented switchable LED strings makes the voltage across the

inductor below V_{LED}.

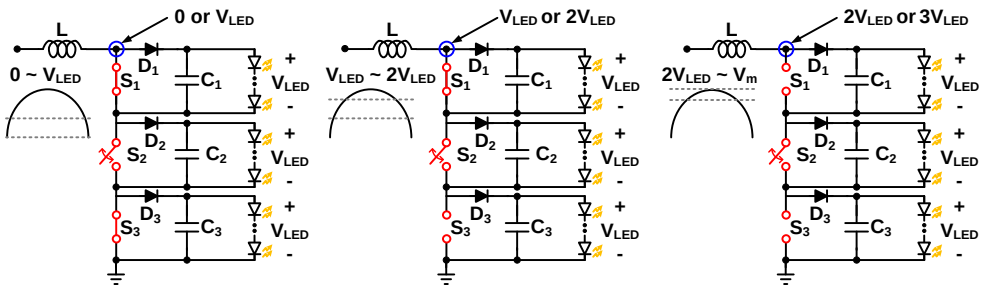

Fig. 3.2. Switching scheme of (a) switching mode 1, (b) switching mode 2, and (c) switching mode 3 in case of N=3.

3.2. Time Division Multiplexing Scheme in *N*-Segmented LED Driver

A time division multiplexing scheme can achieve the current balancing between the LED strings. It has been proposed and its effect was verified in [16] – [17]. Specifically, the DPWM generates switch signal that has the same duty-cycle ratio for N times and each is allocated to every switch from S_1 to S_N sequentially. Fig. 3.3 illustrates the switching timing diagram of the time division multiplexing scheme in each switching mode, in case of N = 3. Assuming that the switching frequency of switch signal (e.g. 135-kHz) is sufficiently high compared to line-period of AC-power source (e.g. 60-Hz), the input voltage at each switching period of S_1, S_2 and S_3 can be considered same during one switching cycle. Note that the switching cycle (1/45k [s]) is the sum of the switching period (1/135k [s]) of S_1, S_2 and S_3. Also, the duty cycle ratios of their switching pulses are also same during one switching cycle. Because these switches are continuously permutated, the time

that each LED strings are connected to charge inductor becomes equal. It is guaranteed due to their same input/output voltage and duty cycle ratio condition. This makes the total charge delivered to each LED string equal in steady-state, which can achieve the current balancing between them.

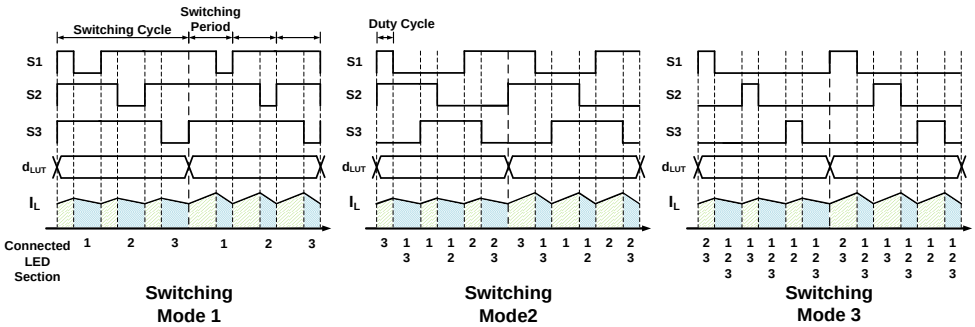

Fig. 3.3. Time-multiplexing scheme of each switching mode in case *N*=3.

3.3. Switch Schedule Allocation

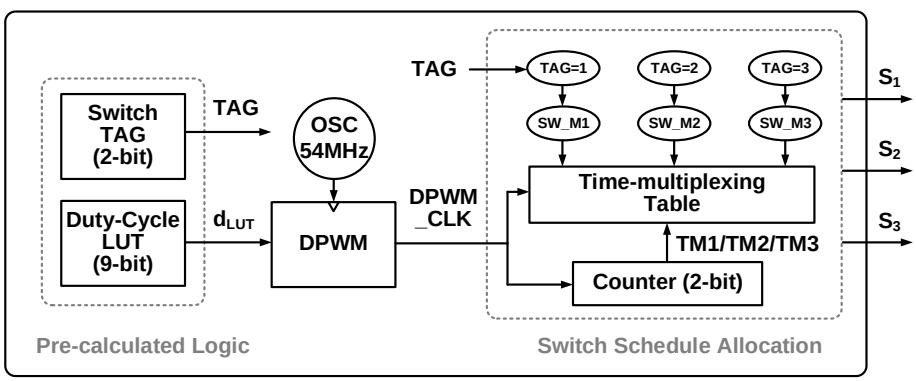

Fig. 3.4. A diagram of switch schedule allocation logic

A switch schedule allocation logic assigns each switch signal depending on a pre-calculated data which consists of duty-cycle ratio and switch *TAG*. The former is required for the PFC and the latter is for reduced inductor voltage as explained in

chapter 2. Fig. 3.4 illustrates the detailed implementation of switch schedule logic. In case of N = 3, the 9-bit optimal duty-cycle codes over time are stored in LUT along with a 2-bit switch *TAG*. According to the value of the 2-bit *TAG*, the switch configuration is determined along with switching modes. For instance, when V_{IN} is in the range from 0 to V_{LED}, the duty-cycle code has *TAG* = 1 that enables the switching mode 1 (i.e. SW_M1). In the same way, SW_M2 and SW_M3 are configured by *TAG* = 2 and *TAG* = 3, respectively. However, this *TAG* value is not fixed and can be changed when the error calibration loop is enabled. For instance, there is the case that the LED driver should operate in SW_M2 (i.e. *TAG* = 2) although V_{IN} is in the range from 0 to V_{LED} to minimize the current error for PFC. The specific operation about variable *TAG* will be described in chapter 4. By using the 9-bit duty-cycle code, the DPWM with an internal oscillator repeatedly generates the same pulse of DPWM_CLK three times. The resolution of the duty-cycle ratio is set by a ratio between 54-MHz oscillator and 135-kHz DPWM_CLK frequencies, of which minimum and maximum duty-cycle are 0 and 400, respectively. By counting the positive edge of DPWM_CLK, the time multiplexing signals (i.e. *TM*1, *TM*2 and *TM*3) are generated, and the one switching switch is selected among S_1, S_2 and S_3.

TABLE 1 summarizes the switching status which is stored in switching schedule logic considering the switching mode and time multiplexing schemes. According to the value of *TAG* and *TM*, the switching schedule logic generates the three scheduled switch signals during each switching cycle that can reduce the

design cost and achieve the current balancing between LED strings.

TAG	TM	S_1	S_2	S_3
1 (SW_M1)	TM1	**DPWM_CLK**	ON	ON
	TM2	ON	**DPWM_CLK**	ON
	TM3	ON	ON	**DPWM_CLK**
2 (SW_M2)	TM1	**DPWM_CLK**	OFF	ON
	TM2	ON	**DPWM_CLK**	OFF
	TM3	OFF	ON	**DPWM_CLK**
3 (SW_M3)	TM1	**DPWM_CLK**	OFF	OFF
	TM2	OFF	**DPWM_CLK**	OFF
	TM3	OFF	ON	**DPWM_CLK**

Table. 3. 1. The switching status in consideration with switching mode and time multiplexing scheme.

Chapter 4
Duty-cycle Control

This chapter describes the duty-cycle control scheme for PFC based on LUT and the error calibration loop. Conventional digitally-controlled AC-DC boost converters [8] – [9], [18] – [20] calculate an appropriate pulse-width at every switching cycle to correct the power factor by sampling three values, such as the rectified AC input, the inductor current and the output voltage. However, such control scheme incurs a lot of computational cost and requires a number of ADCs, which results in both large power consumption and design cost. To address these problem, the LUT-based duty-cycle control scheme is presented that can be simply implemented and correct the power factor without ADC ideally. However, the open-loop duty-cycle control which is based only on LUT incurs a large amount of the input current error and is vulnerable to the non-ideal conditions, such as a output voltage ripple and the voltage variation of V_{IN}. Therefore, the error calibration loop with one current-sampling ADC is employed to mitigate such drawbacks.

4.1. Analysis on Optimal Duty-Cycle Ratio

In this section, the optimal duty-cycle ratio of the switching signal for PFC is derived. In the analysis, the sinusoidal AC voltage source V_{AC} is assumed as

$V_{AC}(t) = V_m \sin \omega t$ for time t, where V_m and ω are magnitude and angular frequency of AC voltage source (i.e. line frequency = 60-Hz), respectively. In addition, the load voltage of each LED string is assumed as a DC voltage of V_{LED}. Fig. 4.1 shows the inductor current waveform at each switching cycle along with corresponding inductor voltage (V_L) and switch state. When the circuit operates in *k*-th switching mode at time $t = t_n$, the differential equations of inductor current can be expressed as (2) and (3).

$$L\frac{di_L(t)}{dt} = V_m \sin \omega t - (k-1)V_{LED} \text{ for } (n-1)T_{SC} \le t < (n-1)T_{SC} + d(t_n)T_{SC} \quad (2)$$

$$L\frac{di_L(t)}{dt} = V_m \sin \omega t - kV_{LED} \text{ for } (n-1)T_{SC} + d(t_n)T_{SC} \le t < nT_{SC} \quad (3)$$

where T_{SC} and $d(t_n)$ represent the period of the switching cycle and the duty-cycle ratio at t_n, respectively. For each switching cycle, the amount of inductor current variation $\Delta i_L(t_n)$ can be derived as (4).

$$\Delta i_L(t_n) = \frac{V_m \sin \omega t_n - (k-1)V_{LED}}{L} \cdot d(t_n) \cdot T_{SC} + \frac{V_m \sin \omega t_n - kV_{LED}}{L} \cdot (1 - d(t_n)) \cdot T_{SC} \quad \cdots (4)$$

The inductor current should follow the pre-calculated ideal reference current I_{ref} for PFC, and the current difference between $I_{ref}(t_n)$ and $I_{ref}(t_{n+1})$ should be equal to $\Delta i_L(t_n)$ as (5).

$$\Delta i_L(t_n) = I_{ref}(t_{n+1}) - I_{ref}(t_n) \quad (5)$$

With (4) and (5), $d(t_n)$ can be derived as (6).

$$d(t_n) = k - \frac{V_m \sin \omega t_n}{V_{LED}} + \frac{L}{V_{LED}T_{SC}}(I_{ref}(t_{n+1}) - I_{ref}(t_n)) \quad (6)$$

Both the optimal duty-cycle ratio and the reference current are stored in LUT.

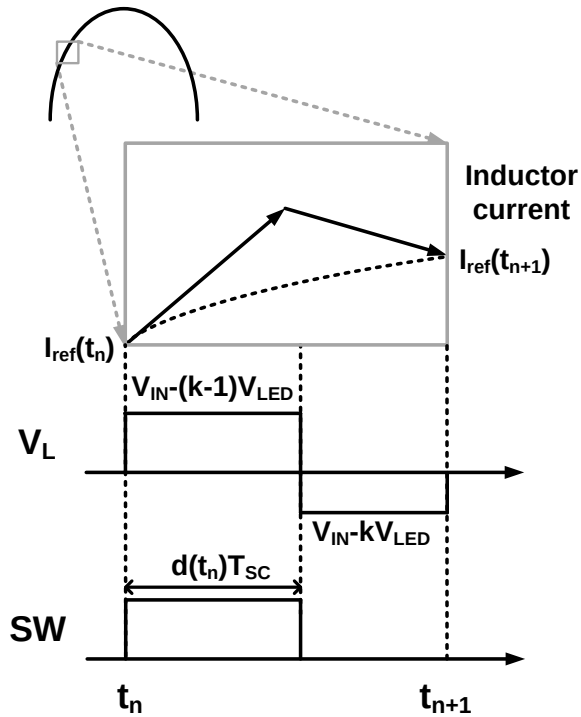

Fig. 4.1. A waveform of inductor current, inductor voltage and switch status at each switching cycle.

Fig. 4.2 plots the simulation results of the theoretical V_{IN}, I_L, and duty-cycle ratio over time. To understand the scheme briefly, the 3-segmented LED driver is simulated based on the open-loop LUT control. The voltage of each LED string (i.e. V_{LED}) is set to 60.8 V. In ideal case, the simulation results show that the pre-calculated duty-cycle ratios from (6) make the input current I_{IN} well matched with I_{ref} that can achieve 99.5 % power factor.

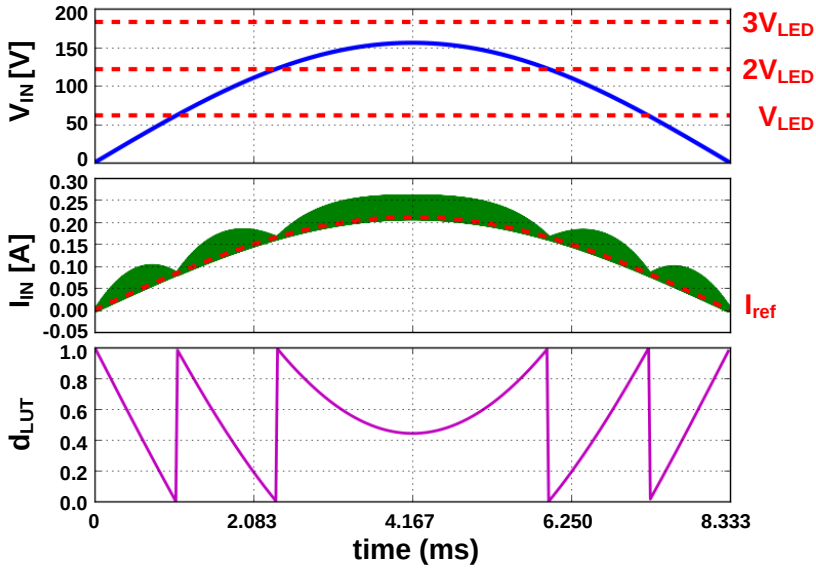

Fig. 4.2. The simulation result of the theoretical V_{IN}, I_L and d_{LUT}.

4.2. Effect on Non-Idealities

The proposed LUT-based open-loop control scheme incurs the large duty-cycle error when the actual design does not meet the aforementioned assumptions. In this subsection, the effect on the input/output voltage disturbance is described.

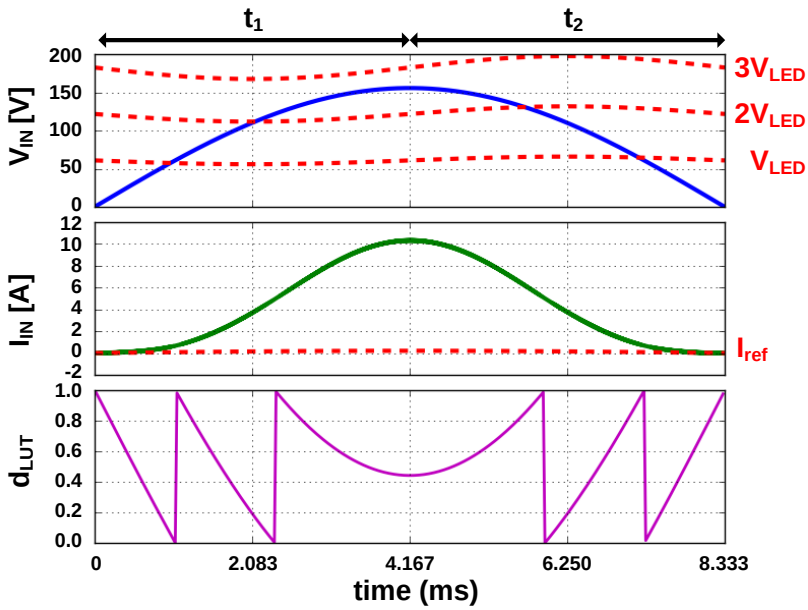

Fig. 4.3. The simulation result of the V_{IN}, I_L and d_{LUT} in case of 10V peak-to-peak V_{ripple}.

First, the load voltage has a voltage ripple due to its finite DC capacitance. Fig. 4.3 shows the simulation waveforms with 10 V peak-to-peak voltage ripple V_{ripple} of V_{LED}. When the finite voltage ripple exists, I_{IN} is not matched with I_{ref}. During t_1, since V_{LED} is smaller than 60.8 V, I_{IN} dramatically increases. In the same way, I_{IN} decreases during t_2, because V_{LED} is larger than 60.8 V. Since the inductor current accumulates each error at every switching timing during whole period, the voltage

ripple can significantly distort the current waveform. Therefore, the excessively large load capacitance is necessary for constant V_{LED} and PFC.

Fig. 4.4 (a) and (b) show the simulation waveforms with positive and negative (e.g. +1 and -1 V) offset voltage of V_{IN}. When the AC-power source has the voltage variation or the finite voltage drop at the rectifying diodes or switches exists, V_{IN} is changed by several voltages. When the offset is positive value, I_{IN} diverges to positive value. On the other hand, when the offset is negative value, I_{IN} diverges to negative value and clamped to zero due to the rectifier. Although the LUT-based predictive control is simple and easy to implement, it is very sensitive to the non-idealities and cannot correct power factor in an actual design.

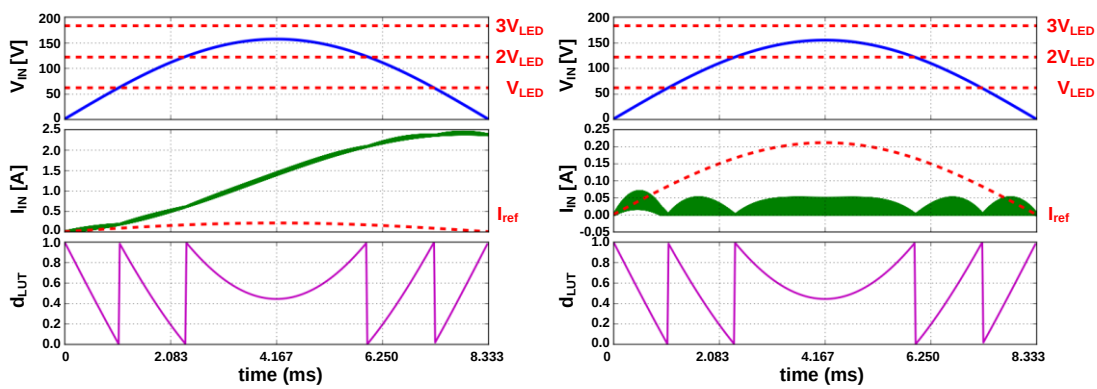

Fig. 4.4. The simulation result of (a) +1 V input voltage offset and (b) -1 V input voltage offset.

4.3. Current Feedback Compensation

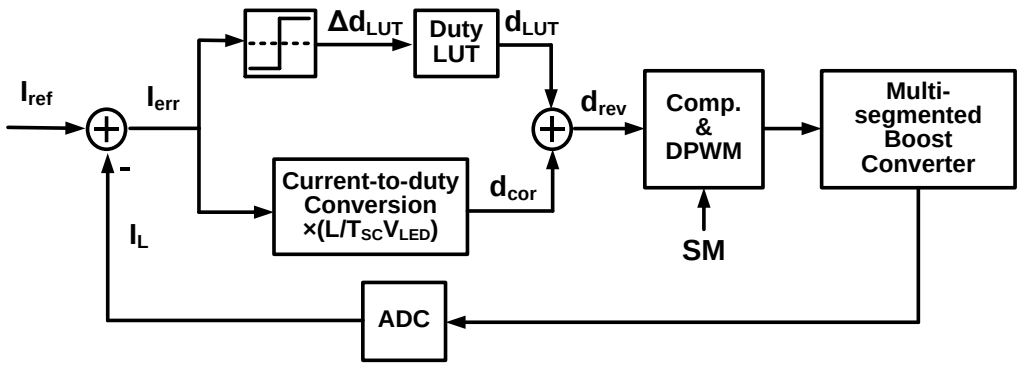

Fig. 4.5. The diagram of current feedback compensation.

In order to alleviate the effect on the non-idealities, the current feedback compensation is presented as shown in Fig. 4.5. The current compensation is performed by correcting the duty-cycle ratio with two feedback loops having different frequencies. One is an instant duty-cycle correction (IDCC) to make the zero current-difference between I_{ref} and I_{IN} at the next switching cycle (i.e. 45-kHz). Specifically, by summing the duty-cycle value in LUT (d_{LUT}) and the correction value (d_{cor}), the revised duty-cycle value d_{rev} can compensate the inductor current error and improve the power factor. The other is a periodic duty-cycle correction (PDCC) that modifies the pre-programmed value in LUT once at every half-line cycle (i.e. 120-Hz). By using a polarity of the current difference (i.e. 1 or -1), the 9-bit duty-cycle value in LUT is updated. In this chapter, the operation principle and implementation issues of both compensation schemes for PFC will be described.

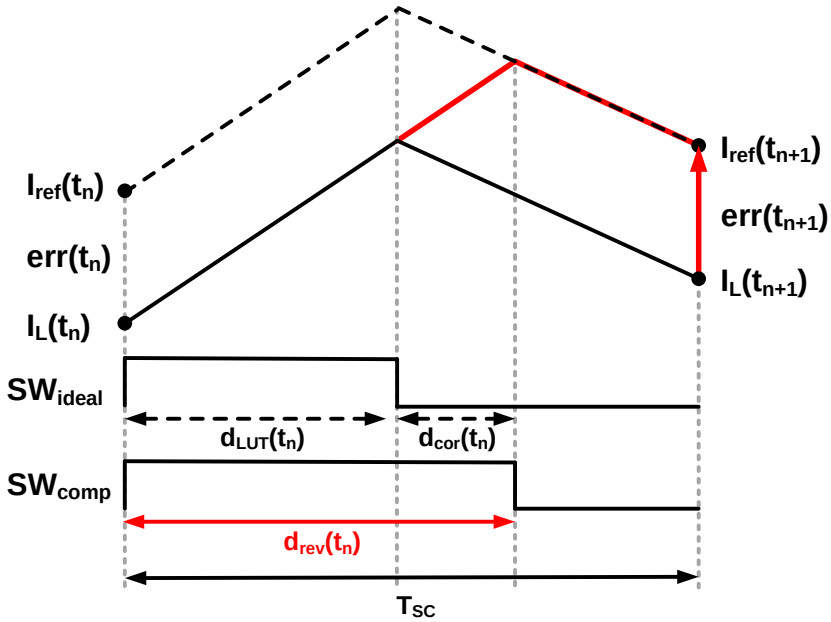

Fig. 4.6. Modifying current status with instant duty-cycle correction.

The strategy for the instant duty-cycle correction scheme is that the subsequent current error, err(t_{n+1}), is compensated by modifying the duty-cycle ratio of right before switching cycle, $d_{\mathrm{LUT}}(t_n)$. Fig. 4.6 illustrates the inductor current waveform and the desired duty-cycle ratio for PFC. Specifically, the next revised duty-cycle ratio $d_{\mathrm{rev}}(t_n)$ can compensate the inductor current error of the current n-th switching cycle by summing the duty-cycle value in LUT (i.e. $d_{\mathrm{LUT}}(t_n)$) and the instant correction value (i.e. $d_{\mathrm{cor}}(t_n)$). From (6), $d_{\mathrm{LUT}}(t_n)$ and $d_{\mathrm{rev}}(t_n)$ can be expressed as (7) and (8), respectively.

$$d_{LUT}(t_n) = k - \frac{V_m \sin \omega t_n}{V_{LED}} + \frac{L}{V_{LED} T_{SC}} (I_{ref}(t_{n+1}) - I_{ref}(t_n)) \tag{7}$$

$$d_{rev}(t_n) = k - \frac{V_m \sin \omega t_n}{V_{LED}} + \frac{L}{V_{LED} T_{SC}} (I_{ref}(t_{n+1}) - I_{IN}(t_n)) \tag{8}$$

By subtracting (7) from (8), the required d_{cor} can be derived as (9).

$$d_{cor}(t_n) = \frac{L}{V_{LED}T_{SC}}(I_{ref}(t_n) - I_{IN}(t_n)) \quad (9)$$

By using the current difference between I_{ref} and I_{IN} at *n*-th switching cycle, the instant correction value d_{cor} at *n*-th switching cycle can be generated that can compensate the error.

In the instant duty-cycle correction scheme, the correction value d_{cor} can make the revised duty-cycle ratio d_{rev} smaller or larger than 0 or 1, which cannot be expressed. For instance, when the output voltage is smaller than the intended constant load voltage (V_{LED}) due to the voltage ripple during t_1, the negative d_{cor} is required, and hence d_{rev} is clamped to 0 around the switching mode transition from SW_M1 to SW_M2 and from SW_M2 to SW_M3. Also, when the output voltage is larger than the intended constant load voltage (V_{LED}) during t_2, the d_{cor} larger than 1 is required, and hence d_{rev} is clamped to 1 around the switching mode transition from SW_M3 to SW_M2 and from SW_M2 to SW_M1. To address this problem, the variable *TAG* is presented as mentioned in chapter 3. By shifting the switching mode as illustrated in Fig. 4.7, the duty-cycle ratio, which is smaller or larger than 0 or 1, can be expressed. In other words, if d_{rev} is negative, (+1) is added to this and switch mode is changed to the adjacent one, and if d_{rev} is over 1, (+1) is subtracted from this and switch mode is changed to the adjacent one. For instance, although V_{IN} is in the range from 0 to V_{LED}, the LED driver operates in SW_M2 by changing the value of *TAG* from 1 to 2. It can be verified with inductor current equation in (4). At SW_M1 (i.e., $k = 1$), the negative duty-cycle ratio (-*d*) can be expressed as (10).

$$\Delta i_L = \frac{V_{IN}}{L} \cdot (-d) \cdot T_{SC} + \frac{V_{IN} - V_{LED}}{L} \cdot (1+d) \cdot T_{SC} = \frac{V_{IN} - V_{LED}(1+d)}{L} \cdot T_{SC} \quad (10)$$

At SW_M2 (i.e. k = 2), the duty-cycle ratio (1-*d*) can be expressed as (11), which is same with (10).

$$\Delta i_L = \frac{V_{IN} - V_{LED}}{L} \cdot (1-d) \cdot T_{SC} + \frac{V_{IN} - 2V_{LED}}{L} \cdot (d) \cdot T_{SC} = \frac{V_{IN} - V_{LED}(1+d)}{L} \cdot T_{SC} \quad (11)$$

In this way, all the corrected duty-cycle ratios can be successfully expressed that can improve the power factor.

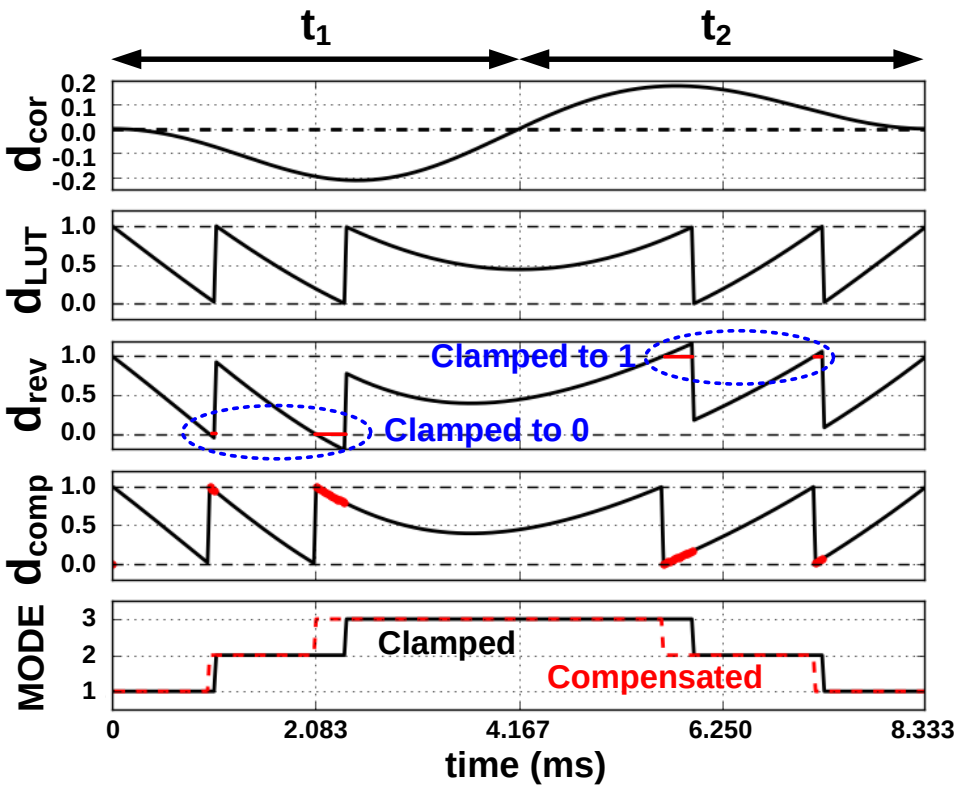

Fig. 4.7. The value of d_{cor}, d_{LUT}, d_{rev} and d_{comp} with switch mode transition and switching mode level for one half-line period.

The strategy for the periodic duty-cycle correction scheme is that the previous duty-cycle code stored in LUT is directly modified by using a 1-bit positive or negative sign of the current inductor current error to compensate the next period's error. Fig. 4.8 illustrates overall periodic duty-cycle correction scheme. This scheme can be referred to as a backward duty-cycle calibration. Since the inductor current error at *k*-th switching cycle, $e(t_k[1])$, is caused by the previous duty-cycle code error at *k*-th switching cycle, $d_k[1]$, updating the previous *k*-th duty-cycle code in LUT can compensate the next line-period's (120-Hz) error at *k*-th switching cycle, $e(t_k[2])$. For instance, when the current inductor current error (i.e. $I_{ref}(t_n)$-$I_{IN}(t_n)$) is positive or negative value, *k*-th duty-cycle code in LUT increments or decrements 1-bit, respectively. This calibration is repeated N_{cal} times for each LUT component and then sequentially progressed from the zero-crossing time to the last time of half-line period. By updating LUT during several periods, each duty-cycle code in LUT moves to the optimal value to keep the power factor close to 1.

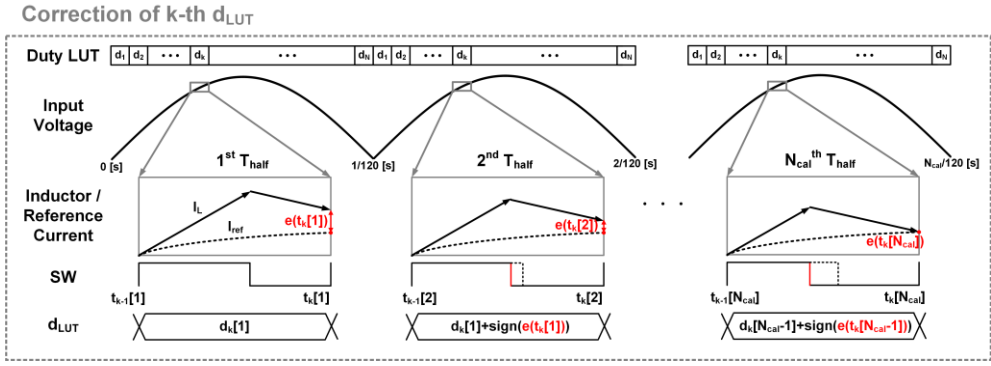

Fig. 4.8. d_{LUT} at *k*-th switching cycle in the middle of the LUT calibration process.

Fig. 4.9 shows the simulation waveforms with both instant and periodic duty-cycle correction schemes. In contrast with Fig. 4.3 and 4.4, the inductor current error is diminished at first, thanks to the instant duty-cycle correction scheme. As periodic duty-cycle calibration progresses, the amount of correcting duty-cycle, d_{cor} diminishes to zero over one half-line period. Finally, the input current I_{IN} converges to I_{ref} that can achieve 99.5 % power factor. Fig. 4.9 shows the progress of two half-line periods of calibration when each LUT component is updated 20 times.

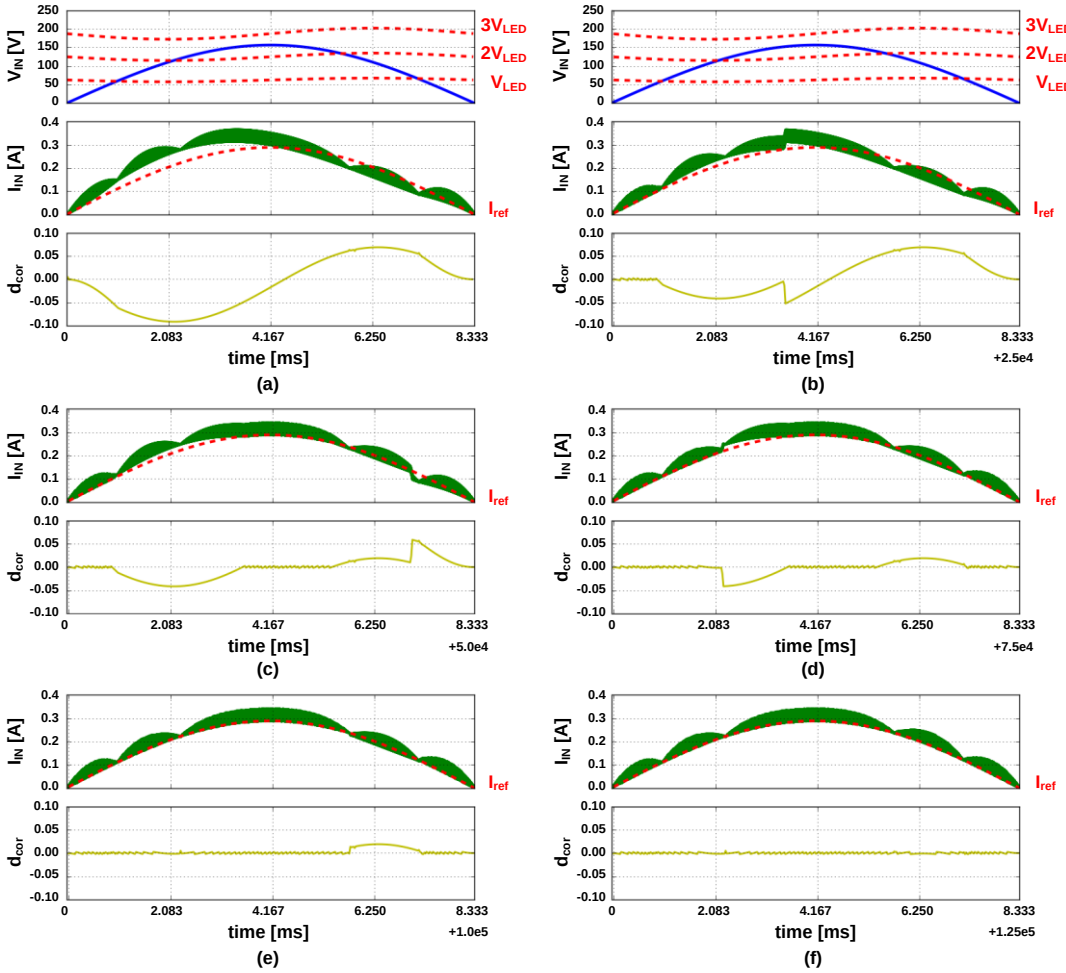

Fig. 4.9. The simulation result of input voltage, current, reference current and duty correction value (d_{cor}) with current feedback compensation (a) at the first half-line period and after calibrating (b) 3000, (c) 6000, (d) 9000, (e) 12000, (f) 15000 times.

Chapter 5
Experimental Results

Fig. 5.1 is a photograph of the prototype LED driver with the 6-segment LED array. Each LED section consists of 19 high-brightness LEDs, and the prototype board is comprised of multiple discrete components, such as an inductor, capacitors, diodes, and transistor switches. Note that opto-coupler gate driver ICs are employed to control the transistor switches using a bootstrapping technique. Also, the proposed digital controller is implemented with a Programmable System-on-Chip (PSoC) evaluation board, a product of Cypress Semiconductor [21]. The measured performance of the proposed LED driver is summarized in Table 5.1. As shown in Fig. 5.2, the proposed LED driver achieved continuous input current waveform and PF in this case was 98.4%. The relationship between the load capacitance and the LED voltage/current is illustrated in Fig. 5.3. It has been experimented when the load capacitance is 22uF, 100uF, 220uF, and 470uF. Fig. 5.3 shows that as the capacitance increases, the ripple of LED voltage and current becomes far reduced.

Moreover, PF and efficiency of the proposed LED driver were measured according to the average current level of the LED sections as plotted in Fig. 5.4. The maximum PF was 98.9%, and the maximum efficiency was 95.6% including the power consumption of the PSoC board. Additionally, harmonic components of

the input current were evaluated to test if the implemented LED driver satisfies IEC 61000-3-2 standard. As plotted in Fig. 5.5, harmonic components normalized to 1st harmonic (60 Hz) component is below the IEC 61000-3-2 skirt, which is the strong point against the previous works [3] – [4] in that a costly EMI filter is unnecessary.

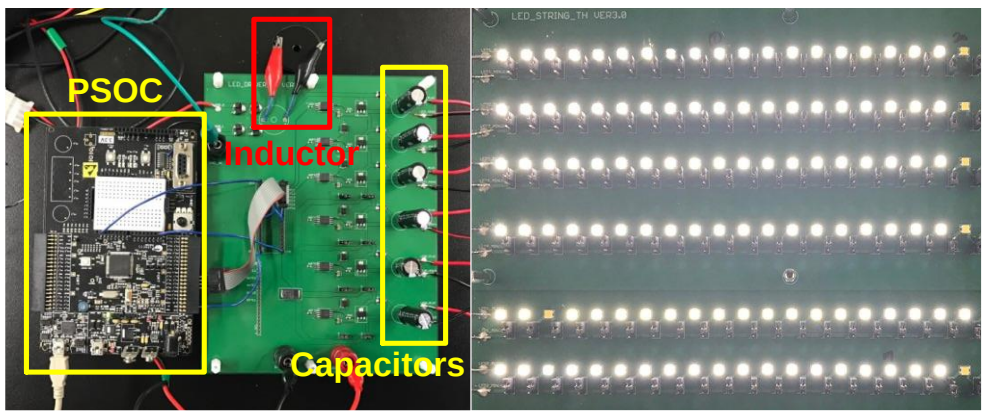

Fig. 5.1. The prototype of the proposed multi-segmented LED driver and the LED array.

Parameter	Value
Input voltage (V_{AC})	220 V_{RMS} (60Hz)
LED string voltage (V_{LED})	52 ~ 60 V
Number of segments	6
Switching frequency (f_{SW})	135 KHz
Switching cycle frequency(f_{SC})	22.5 KHz
Number of LEDs per string	17 ~ 20
Max. power factor	99.6 %
Max. power efficiency	95.6 %
Max. LED current	209 mA
Max. current balance error	3.1 %

Table. 5.1. The measured performance of the proposed LED driver.

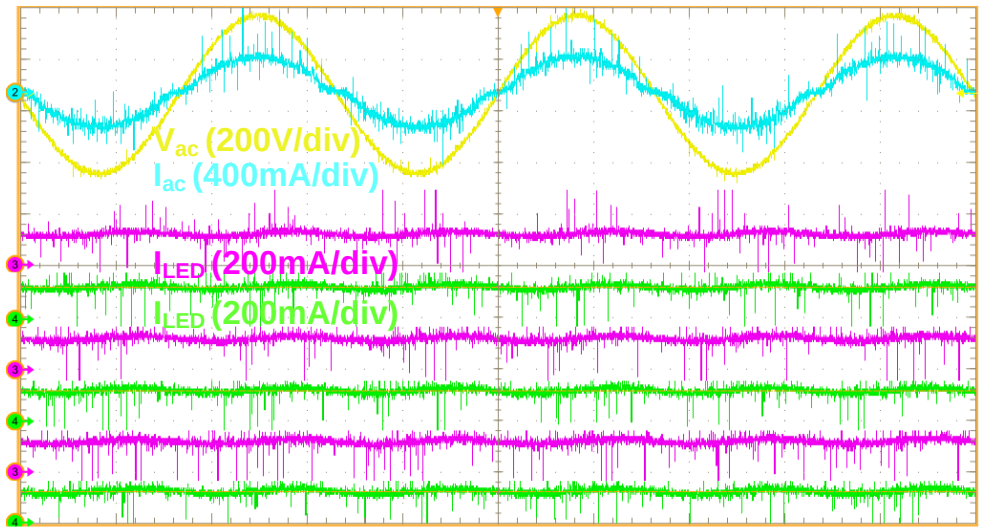

Fig. 5.2. The measured input voltage (V_{ac}), current (I_{ac}) and each LED channel current (I_{LED}).

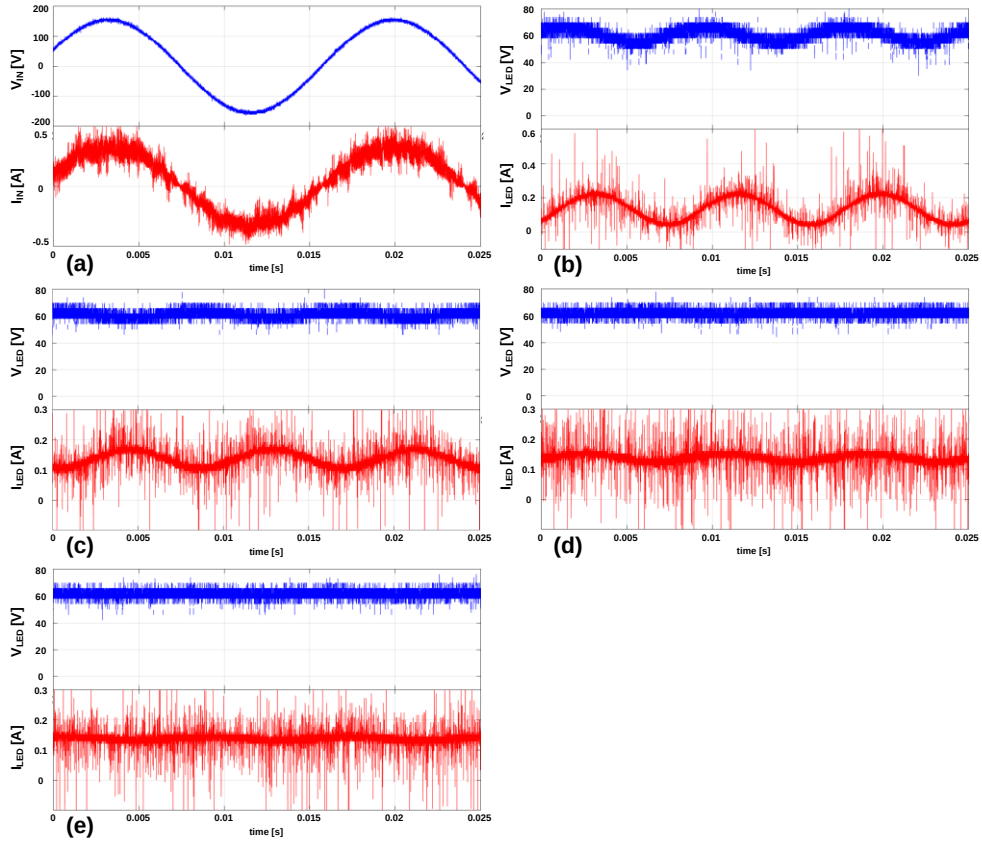

Fig. 5.3. The measured waveform of (a) input voltage (V_{IN}), input current (I_{IN}), and the LED voltage (VLED), LED current (ILED) when the load capacitance is (b) 22uF, (c) 100uF, (d) 220uF, and (e) 470uF.

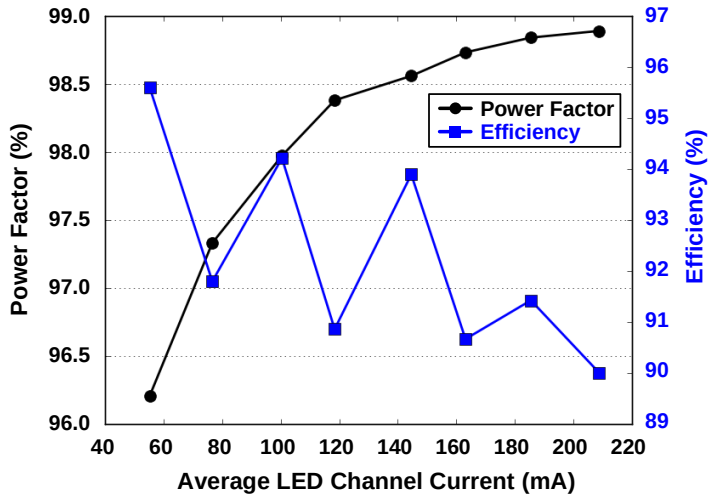

Fig. 5.4. The measured power factor and conversion efficiency of the prototype LED driver according to the average LED channel current.

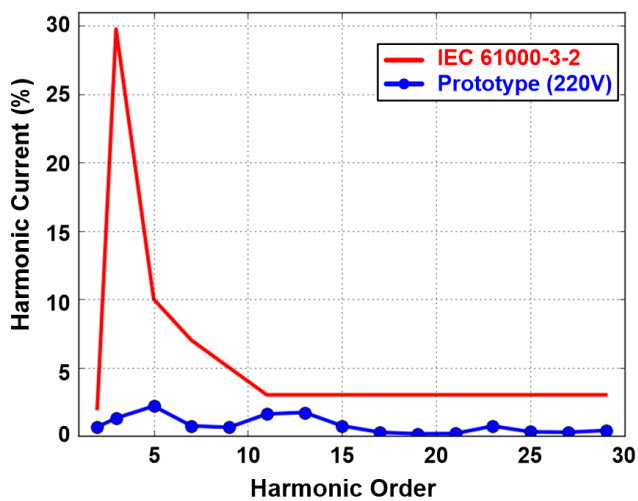

Fig. 5.5. Harmonic component of the input current and IEC 61000-3-2 skirt.

To assure the robustness of the proposed LED driver, this thesis compares the results with and without the proposed digital control schemes. First, by setting the initial LUT configuration anticipating the constant load voltage, we observe the input current waveforms. Fig. 5.6 (a) is the case without the proposed LUT calibration and switching scheme with the proposed controller. Fig. 5.6 (b) is the case only with the LUT calibration process. Lastly, Fig. 5.6 (c) is the case with the proposed LUT calibration and switching scheme. Since the load voltage has a ripple of several volts, the current waveform of Fig. 5.6 (a), (b) exhibits distortion and shows 94.6%, 94.3% PF, respectively, in comparison with the result of Fig. 5.6 (c) with 98.4% PF. Fig. 5.7 shows the periodic current error occurring at each switching cycle (T_{SC}=1/45k [s]) during one half-line period. When the LED sections are controlled only with the previous LUT-based control [2], the maximum current error for one half-line period peaks around 460mA. If only the LUT calibration is applied, the fore part of current error diminishes to zero. However, there are still multiple spike-like error profiles across the half-line period. Finally, with the LUT calibration and switching mode selection scheme, overall current error during one half-line period converges to zero and the consequent RMS and peak current error are 26mA$_{rms}$ and 110mA, respectively.

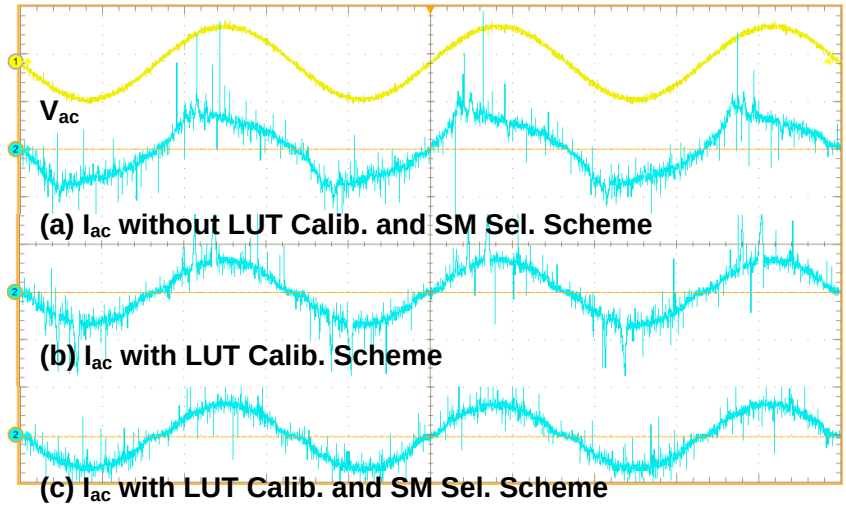

Fig. 5.6. The input current waveforms (a) without the LUT calibration and the switching mode selection scheme, (b) only with the LUT calibration scheme and (c) with the both schemes.

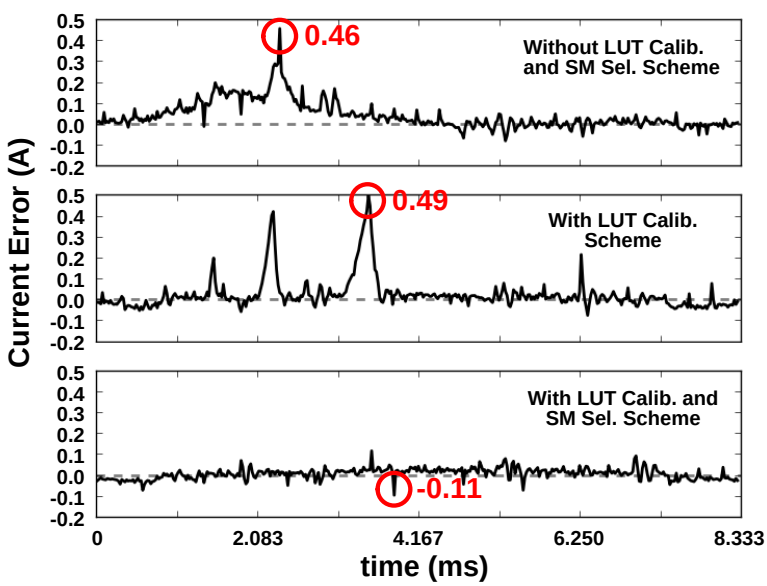

Fig. 5.7. The measured current error detected by the ADC for one half-line period.

Chapter 6
Conclusion

This thesis presented the LUT-based digital control scheme for the AC-powered, multi-segmented LED driver. To use boost converter-based topology as a competitive LED driver, in that, it can reduce component cost of driver itself and be free from bulky input EMI filter, a LED string is divided into several sections in series. A predictive control is employed to switch and synchronize multiple switches sophisticatedly. Several sets of LUT helps LED driver maintaining high power factor and accurate input current even if in highly non-linear switching condition. In addition, adopting the background LUT calibration and the flexible switching mode selection methods guarantee more stable PFC operation and high quality performance even if several volts of load voltage ripples and unexpected temperature changes are accompanied. The cost analysis suggested a way to figure out the optimal number of LED segments in multi-segmented LED driver, and the measurement results demonstrated high power factor, conversion efficiency, and robustness against the ambient environment condition.

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초 록

엘이디를 이용한 조명은 조명시장에서 점차 주요한 비중을 차지하고 있으며, 또한 미국의 에너지부와 같은 세계적인 에너지 관련 기관들의 도움을 받고 있다. 이것은 엘이디가 기존의 조명에 비해 전기-빛 전환효율이 높기 때문에, 조명을 엘이디로 대체하였을 경우 세계의 에너지 소비를 크게 줄일 수 있기 때문이다. 하지만 보다 빠른 엘이디의 사용증가를 위해서 가격이 낮고 신뢰도가 높은 드라이버가 필요하다.

이 논문은 교류입력을 받는 부스트 컨버터 기반의 다중 분할 엘이디 드라이버에 대해 설명한다. 이 드라이버는 룩업테이블을 이용하는 디지털 예측 제어방식과 룩업테이블의 백그라운드 교정기술을 이용해서 높은 역률과 정확한 입력 전류 크기를 얻는다. 제안된 다중 분할 엘이디 드라이버는 로드 단의 엘이디를 여러 개의 직렬 연결된 구획으로 나눔으로써 높은 전압을 견디는 캐패시터, 큰 인덕턴스를 갖는 인덕터가 차지하던 비용을 줄였다. 하지만 제어해야하는 스위치의 수가 늘어남에 따라 보다 정교한 제어 방식이 필요하며, 이는 보다 신속하게 스위칭 모드를 바꾸고 환경변화에 적응하는 것을 요구한다.

제안된 엘이디 드라이버는 이 문제를 룩업테이블을 사용함으로써 해결한다. 룩업 테이블에는 예측된 상황에 대한 정보가 저장되어있으며, 그 결과 220-V 교류 입력에 대해 빠른 대응을 할 수 있다. 또한 주기적인 백그라운드 교정기술과 최적화된 스위치 모드 선택 방식을 통해 예상치 못한 환경적인 변화에 대응할 수 있다. 프로토타입 엘이디 드라이버는 6개의 구획을 가지며, 38.3-W의 입력 전력 하에서 98.4%의 역률과 91%의 전환효율을 보이고 이산소자 가격을 67% 줄이는데 성공하였다.

주요어 : 교류입력 엘이디 드라이버, 예측 제어, 룩업테이블, 부스트 컨버터, 분할방식, 백그라운드 교정기술

학 번 : 2014-22575